a latch circuit for receiving and holding a desired programming state of an associated programmable element, said plurality of element programming circuits setting the state of said associated programmable elements in accordance with a desired programming state held in an associated latch in response to a common control signal; and

A1 Cancel.

a latch programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal, said latch programming circuit comprising,

a latch isolation transistor coupled between said programmable element and said latch circuit, and

a latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through said latch isolation transistor.

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7. A programming circuit for a programmable element, comprising:

A2

at least one latch circuit;

at least one latch-programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal;

a signal line applying a voltage sufficient to change the state of said programmable element;

at least one latch isolation transistor coupled between said programmable element and said latch circuit;

at least one state control transistor coupled between said programmable element and a first reference voltage and having a gate controlled by an output of said latch circuit;

wherein said at least one latch-programming circuit further comprises, at least one latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through one of said at least one latch isolation transistor, and

wherein during a programming phase, said latch circuit is configured to latch said programming signal, and during a common control phase, said latch isolation transistor is configured to decouple said programmable element from said latch circuit and said signal line is configured to apply said state-changing voltage to said programmable element if said output of said latch circuit turns on said state control transistor.

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~~16.~~ A memory circuit, comprising:

a plurality of memory elements; and

at least one programming circuit associated with a plurality of programmable elements and configured to activate one or more of said plurality of memory elements, said programming circuit comprising:

a plurality of programmable elements;

a plurality of element programming circuits each associated with a programmable element and each including

a latch circuit for receiving and holding a desired programming state of an associated programmable element, said plurality of element programming circuits setting the state of said associated programmable elements in

accordance with a desired programming state held in an associated latch in response to a common control signal; and

A3 Cancel.

a latch programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal, said latch programming circuit comprising,

a latch isolation transistor coupled between said programmable element and said latch circuit, and

a latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through said latch isolation transistor.

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~~21~~. A memory circuit, comprising:

a plurality of memory elements; and

AP

at least one programming circuit associated with a plurality of programmable elements and configured to activate one or more of said plurality of memory elements, said programming circuit comprising:

at least one latch circuit;

at least one latch-programming circuit for temporarily applying a programming signal to an input of a respective latch circuit, said latch circuit latching a state of said programming signal;

a signal line applying a voltage sufficient to change the state of said programmable element;

at least one latch isolation transistor coupled between said programmable element and said latch circuit;

at least one state control transistor coupled between said programmable element and a first reference voltage and having a gate controlled by an output of said latch circuit;

A4 cont

wherein said latch-programming circuit comprises at least one latch-programming transistor having a gate controlled by a first latch-programming signal, a first source/drain coupled to a second latch-programming signal, and a second source/drain coupled to said input of said latch circuit through one of said at least one latch isolation transistor;

wherein during a programming phase, said latch circuit is configured to latch said programming signal, and during a common control phase, said latch isolation transistor is configured to decouple said programmable element from said latch circuit and said signal line is configured to apply said state-changing voltage to said programmable element if said output of said latch circuit turns on said state control transistor.